

APPENDIX

Issued Patents

| Line No. | Patent Number | Title | Issue Date | Recordation Information |
|----------|---------------|---|-------------------|---|
| 1. | 7,017,064 | Calculating Apparatus Having A Plurality Of Stages | March 21, 2006 | <p>Reel/Frame: 011800/0442 Assignors: THOMAS, Terence Neil and DAVIS, Stephen J. Assignee: CHRYSALIS-ITS INC.</p> <p>Reel/Frame: 012912/0547 Assignors: CHRYSALIS-ITS INC Assignee: MOSAID TECHNOLOGIES, INC.</p> <p>Reel/Frame: 021040/0648 Assignors: MOSAID TECHNOLOGIES, INC. Assignee: SATECH GROUP A.B. LIMITED LIABILITY COMPANY</p> |
| 2. | 5,469,401 | Column Redundancy Scheme For Dram Using Normal And Redundant Column Decoders Programmed With Defective Array Address And Defective Column Address | November 21, 1995 | <p>Reel/Frame: 006197/0730 Assignors: GILLINGHAM, Peter B. Assignee: MOSAID TECHNOLOGIES, INC.</p> <p>Reel/Frame: 021040/0648 Assignors: MOSAID TECHNOLOGIES, INC. Assignee: SATECH GROUP A.B. LIMITED LIABILITY COMPANY</p> |
| 3. | 5,708,619 | Column Redundancy Scheme For Dram Using Normal And Redundant Column Decoders Programmed With Defective Array Address And Defective Column Address | January 13, 1998 | <p>Reel/Frame: 021040/0633 Assignors: GILLINGHAM, Peter B. Assignee: MOSAID TECHNOLOGIES, INC.</p> <p>Reel/Frame: 021040/0648 Assignors: MOSAID TECHNOLOGIES, INC. Assignee: SATECH GROUP A.B. LIMITED LIABILITY COMPANY</p> |
| 4. | 5,546,343 | Method And Apparatus For A Single Instruction Operating Multiple Processors On A Memory Chip | August 13, 1996 | <p>Reel/Frame: 008489/0485 Assignors: ELLIOTT, Duncan and SNELGROVE, Martin Assignee: MOSAID TECHNOLOGIES, INC.</p> <p>Reel/Frame: 020837/0596 Assignors: ELLIOTT, Duncan Assignee: MOSAID TECHNOLOGIES, INC.</p> <p>Reel/Frame: 020837/0985 Assignors: SNELGROVE, Martin Assignee: MOSAID TECHNOLOGIES, INC.</p> <p>Reel/Frame: 021040/0648 Assignors: MOSAID TECHNOLOGIES, INC. Assignee: SATECH GROUP A.B. LIMITED</p> |

| | | | | |
|----|-----------|---|-------------------|---|
| | | | | LIABILITY COMPANY |
| 5. | 6,560,684 | Method And Apparatus For An Energy Efficient Operation Of Multiple Processors In A Memory | May 6, 2003 | Reel/Frame: 020837/0596 Assignors: ELLIOTT, Duncan Assignee: MOSAID TECHNOLOGIES, INC. Reel/Frame: 020837/0985 Assignors: SNELGROVE, Martin Assignee: MOSAID TECHNOLOGIES, INC. Reel/Frame: 021040/0648 Assignors: MOSAID TECHNOLOGIES, INC. Assignee: SATECH GROUP A.B. LIMITED LIABILITY COMPANY |
| 6. | 7,155,581 | Method And Apparatus For An Energy Efficient Operation Of Multiple Processors In A Memory | December 26, 2006 | Reel/Frame: 020837/0596 Assignors: ELLIOTT, Duncan Assignee: MOSAID TECHNOLOGIES, INC. Reel/Frame: 020837/0985 Assignors: SNELGROVE, Martin Assignee: MOSAID TECHNOLOGIES, INC. Reel/Frame: 021040/0648 Assignors: MOSAID TECHNOLOGIES, INC. Assignee: SATECH GROUP A.B. LIMITED LIABILITY COMPANY |

APPENDIX

Pending Applications

| Line No. | Application Number | Title | Filing Date | Recordation Information |
|----------|--------------------|--|-----------------|---|
| 7. | 11/327725 | Calculating Apparatus Having A Plurality Of Stages | January 6, 2006 | <p>Reel/Frame: 021053/0286 Assignors: THOMAS. Terence Neil and DAVIS, Stephen J. Assignee: CHRYSALIS-ITS INC.</p> <p>Reel/Frame: 021053/0396 Assignors: CHRYSALIS-ITS INC Assignee: MOSAID TECHNOLOGIES, INC.</p> <p>Reel/Frame: 021040/0648 Assignors: MOSAID TECHNOLOGIES, INC. Assignee: SATECH GROUP A.B. LIMITED LIABILITY COMPANY</p> |